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RESEARCH ARTICLE

Low power three-stage OTA using reverse nested frequency compensation without nulling resistor

Vaibhav*, Raj K. Tiwari

Abstract

This study introduces a novel reverse nested miller compensated high gain three-stage operational transconductance amplifier (OTA) that exhibits lower power consumption and maximum allowable voltage swing. In this context, two amplifiers have been employed. The initial amplifier employs PMOS as the primary amplifying component, with a specified I_{DD} value of 200 nA. In the subsequent stages, the second and third amplifiers are biased to operate at a current 2 times I_{DD}. These operations are conducted within a 45 nm cadence virtuoso environment. The other three-stage amplifier employs PMOS as the primary amplifier, with a bias current (I_{DD}) of 4 µA. In a 90 nm cadence virtuoso environment, both the second and third stages are biased to operate at a current of 5 times I_{DD}. The primary design criteria introduced in this design approach are gain, phase margin, and power consumption, which are thoroughly stated. The circuits undergo Monte Carlo and corner evaluations, and the findings are deliberated about in the conclusion of the research. In order to attain the greatest allowable voltage swing, these amplifiers are fabricated with V_{DD} values of 500 and 900 m. The output voltage is set to a constant value of $V_{DD}/2$.

Keywords: Low power, Three stages, Reverse nested miller compensation, Without nulling resistor

Introduction

The operational transconductance amplifier (OTA) is common in mixed-mode and analog circuits. The intrinsic gain of metal-oxide-semiconductor field-effect transistors (MOSFETs) is reduced due to enhanced complementary metal-oxide-semiconductor (CMOS) technology and the reduction in component size, whereas the industry trend is towards higher frequency and resolution. Therefore, the necessity for high-gain and high-speed OTA is inevitable (*Pude, M., et al. 2007*), (*Fordjour et al., 2020*). As a result, research on the design problems with multistage amplifiers is still ongoing (*Nguyen, R., 2010*), (*Giustolisi, G, 2017*), (*Ranjbar, E. 2017*), (*Riad, J., 2019*),(*Fordjour et al., 2020*). To deal with this issue, two main strategies are suggested. More high-gain and high-speed OTAs are intended to be implemented using cascode and cascade setups. The cascode approach is suitable for high supply voltages because the cascode transistor limits output swing. However, cascade and multistage OTAs function better in low-voltage applications. Because of higher number of poles and zeros, this approach requires additional power dissipation and must be adjusted. In order to avoid stability problems and obtain a sufficient phase margin (PM), the major focus of multistage amplifier design is to conduct adequate frequency compensation (*Biabanifard, S., 2018*).

In multistage amplifiers, complicated frequency compensation schemes are required for the closed-loop stability criterion. This discussion centers around two arrangements, namely nested Miller compensation and reverse nested Miller compensation, which are commonly employed in the compensation frequency of three-stage amplifiers. (*Eschauzier,1995*). The nested Miller compensation technique and its numerous variations (*You, F., Embabi,1997*), (*Leung, K.N. 2001*), (*Peng, X. 2002*), (*Ramos, J. 2004*), (*Peng, X. 2005*), (*Grasso, A.D., 2007*) the amplifier is characterized by its slow response and high power consumption, necessitating the use of compensation capacitors that are proportional to the load. (*Leung, K.N., 2001*), (*Fordjour et al., 2020*), rendering such a structure unsuitable for our intended application. The load capacitor and the compensation capacitor load the output node in the NMC structure, producing a more dominant pole. Regarding GBW, this problem reduces frequency response (*Biabanifard, S., 2018*).

Department of Physics and Electronics, Dr RML Awadh University, Ayodhya, Uttar Pradesh, India.

***Corresponding Author:** Vaibhav, Department of Physics and Electronics, Dr RML Awadh University, Ayodhya, Uttar Pradesh, India, E-Mail: vaibhav43309@gmail.com

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Another popular compensation method for multistage amplifiers is reverse nested frequency compensation (RNMC). The non-dominant poles can be separated from the dominant poles in order to get a greater distance from unity gain frequency. Utilization of the Miller capacitance is employed. Although RNMCs have good stability, they use more power and have very little bandwidth. The RNMC was essentially developed to circumvent the output load capacitor issue that plagues the nested miller approach (*Palumbo, G. 2002), (Eschauzier, 1995*). Since the compensation capacitances are not loaded on the output nodes, RNMC often has low power requirements and greater bandwidth.

Design Techniques

The initial stage in constructing the compensation network involves doing an analysis of the open loop transfer function for the specified topology. The analysis can be conducted by evaluating the small-signal circuits that are equivalent. In these circuits, the parameters G_{mi}, R_{oi}, and C_{oi} represent the ith stage's transconductance, resistance, and equivalent output capacitances, respectively. Additionally, C_L denotes the load capacitance. The transfer function will be executed under the premise that the closed-loop gain (C_L), the capacitance values of C_{C1} and C_{C2}, are considerably greater than the output capacitance (C_{oi}). Additionally, it is assumed that the gain of each stage (Avi = Gmi Roi) is significantly greater than one to maintain accuracy while simplifying the calculation. The higher frequency poles will be disregarded because of the presence of parasitic capacitances (*Grasso, A.D., 2007*)

The capacitive feedback loop stabilizes the amplifier in reverse nested Miller compensation by supplying negative feedback. Capacitive feedback, however, indicates an internal loading within the amplifier. Because the feed-forward current *via* these compensation capacitors is out of phase with the current entering the loading capacitor, the feed-forward effect they produce results in a right half plane (RHP) zero (*R. Mita, G,2001*). In response to this finding, we included a nulling resistor. The nulling resistor blocks the feed-forward routes. As a result, it can prevent the compensating capacitor from rapidly pulling down the first stage form's output impedance. As a result, the nulling resistor decreases the first stage gain drops at high frequency, increasing the phase margin. (*Ho, K.P., 2003*). Although in this particular paper the RNMC structure is adopted is conceptually same as suggested in (*Grasso, A.D.,2007), (Grasso, A.D.,2010*) with a similar open loop transfer function and amplifier topology, but the difference in technology and implementation by putting value of nulling resistor $R_C = 0$. This RNMC structure is designed for low supply voltage, lower power consumption and maximum allowable voltage swing.

$$\omega_{p1} \cong \frac{1}{C_{c1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3}} \quad (1)$$

$$A_0 = -g_{m1} r_{01}\, g_{m2} r_{02} g_{m3} r_{03} \quad (2)$$

Where A_0 is the Gain

Therefore, the GBW is

$$\omega_{GBW} = |A_0|\, \omega_{p1} = \frac{g_{m2}}{C_{C1}} \quad (3)$$

$$g_{mvf} = g_{m8} \quad (4)$$

In order to attain a push pull O/P stage after simplification A_{VS} is as mentioned in (*Grasso, A.D.,2010*) without nulling resistor R_C.

$$A_{VS} = \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)} \frac{1 + S\left[\frac{C_{C2}}{g_{m6}}\left(\frac{g_{mvf}}{g_{m8}} - 1\right) + \frac{C_{C1}}{g_{m6}\, g_{m8}\, R_{02}}\right] - S^2 \frac{C_{C1} C_{C2}}{g_{m6}\, g_{m8}}}{1 + S\left[\frac{C_L C_{C2}}{g_{m8} C_{C1}} + \frac{C_{C2}}{g_{m8}} + \frac{C_{C2}}{g_{m6}} \frac{(g_{mvf} - 1)}{g_{m8}}\right] + S^2 \frac{C_{C2} C_L}{g_{m6} g_{m8}}} \quad (5a)$$

Now putting (4) into (5a)

$$A_{VS} = \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)} \frac{1 + S\frac{C_{C1}}{g_{m6}\, g_{m8}\, R_{02}} - S^2 \frac{C_{C1} C_{C2}}{g_{m6}\, g_{m8}}}{1 + S\frac{C_L C_{C2}}{g_{m8} C_{C1}} + S^2 \frac{C_{C2} C_L}{g_{m6} g_{m8}}} \quad (5b)$$

The design process typically begins with determining the system's transconductance for first stage g_{m1}, g_{m2}, which is selected to satisfy the random offset's noise requirement or standard deviation due to mismatches. Subsequently, the value of C_{C1} is acquired by establishing the necessary gain bandwidth product. The setting of C_{C2} is determined to mitigate the presence of peaks in the frequency response.

The rightmost estimate is valid if $C_L >> C_{C1}$ It is worth noting that unlike other compensation techniques (*Grasso, A.D., 2007*) (*Leung, K.N., 2001)* where C_{C2} is directly proportional to C_L. The C_{C2} method is predicated on the assumption of small values when strong capacitive loads are present, resulting in a significant reduction in silicon area. Moreover, in contrast to typical NMC topologies, where a greater gm6 value is considered preferable for amplifier performance, the transconductance value of the last stage is determined to achieve practical values for C_{C2}.

For the sake of achieving simplicity among all the solution it is conceivable we set (*Grasso, A.D.,2010*).

$$\emptyset = \tan^{-1} \frac{G_{NM2}\, C_{C1}{}^2 - G_{NM1}{}^2 C_L C_{C2}}{G_{NM1} G_{NM2} C_L C_{C2}} \quad (6)$$

Where $G_{NM1} = \frac{g_{m2}}{g_{m8}}$ and $G_{NM2} = \frac{g_{m6}}{g_{m8}}$

To maintain asymptotic stability, the transconductance of the second stage must be significantly greater than that of the first stage. Finally, it should be observed that, in contrast to NMC g_{m8}, the variable in question has the potential to take on any value, regardless of its convenience, including values that are less than g_{m2}.

Further,

$$FOM_S = \frac{\omega_{GBW} C_L}{power} \quad (7)$$

$$IFOM_S = \frac{\omega_{GBW} C_L}{I_{DD}} \quad (8)$$

The simplified schematic (1) of three stages OTA is realized and implemented in this paper using 45 and 90 nm

cadence virtuoso environment. This paper is an adaptation of (*Grasso, A.D., 2007)* and (*Grasso, A.D., 2010*).The three stage OTA is simulated under cadence virtuoso environment by fixing output level at $V_{DD}/2$ so that to provide maximum voltage allowable voltage swing, by doing so we are getting overall better response, for frequency compensation RNMC methodology is used by using two compensation capacitor i.e. C_{C1} and C_{C2}, $C_L >> C_{C2}$ and comparable to C_{C1}.

The initial phase consists of a PMOS differential pair, denoted as Q1-Q2, and a current mirror load, represented as Q3-Q4. The second stage is implemented as an inverting stage using transistors Q5 and Q6, while the final inverting stage consists of transistors Q7 through Q10. The feed-forward stage of the g_{mvf} is created by utilizing the active load transistor Q10 from the previous stage, where its gate is coupled to the output of the first stage. Furthermore, in this configuration, Q9 and Q10 function as a pseudo class AB output stage that is capable of driving the load capacitor C_L.

First parameter sets for p type OTA in 45 nm environment for V_{DD} of 500 mv and I_D of 200nA for $g_{m1=}$ g_{m2}= 2.77 $\mu A/V$ and C_{C1}= 1.5 pF. Then, to obtain phase margin around 60^0 we set g_{m6}= 13.86 $\mu A/V$. We set $g_{m6=}$13.86 $\mu A/V$ $g_{m8=}$15.48 $\mu A/V$ $g_{m10=}$14.3 $\mu A/V$. The compensation capacitor C_{C2} was ultimately adjusted to a value of 0.4 pF through computer simulation. Similarly, the compensation capacitors C_{C1} and C_{C2} were fine-tuned to 1.5 and 0.4 pF, respectively. The drain current of Q1 and Q2 was set to 100 nA, while the drain current of the second and third stages reached 400 nA, resulting in a total current consumption of 1.4 µA. The dimensions of transistors are presented in Table 1. Figure 1 illustrates the simulated open loop frequency response of the amplifier. The DC gain is measured to be 77.9 (dB). The gain-bandwidth product was measured to be 0.610 KHz, while the phase margin was determined to be 60.78^0.

Second parameter sets for p-type OTA in 90 nm environment for V_{DD} of 900 mv and I_D of 4A $\mu g_{m1=}$ g_{m2}= 30.747 $\mu A/V$ and C_{C1}= 2pF. Then, to obtain phase margin around 60^0 we set g_{m6}=111.179 $\mu A/V$. we set $g_{m6=}$111.179 $\mu A/V$ $g_{m8=}$123.46 $\mu A/V$ $g_{m10=}$144.352 $\mu A/V$. The compensation capacitor C_{C2} was ultimately adjusted to a value of 0.48 pF. The compensation capacitors CC1 and CC2 were fine-tuned through computer simulation to 2 and 0.5 pF, respectively. This adjustment

Table1(a): Transconductance

Transconductance	*45 nm*
g_{m0}	5.33
g_{m1},g_{m2}	2.77
g_{m3},g_{m4}	2.89
g_{m5}	12.89
g_{m6}	13.86
g_{m7},g_{m9}	14.27
g_{m8}	15.48
g_{m10}	14.3

Table1(b): Transconductance

Transconductance	*90 nm*
g_{m0}	62.25
g_{m1},g_{m2}	30.7149
g_{m3},g_{m4}	12.52
g_{m5}	253.005
g_{m6}	111.89
g_{m7},g_{m9}	229.9
g_{m8}	127.92
g_{m10}	158.55

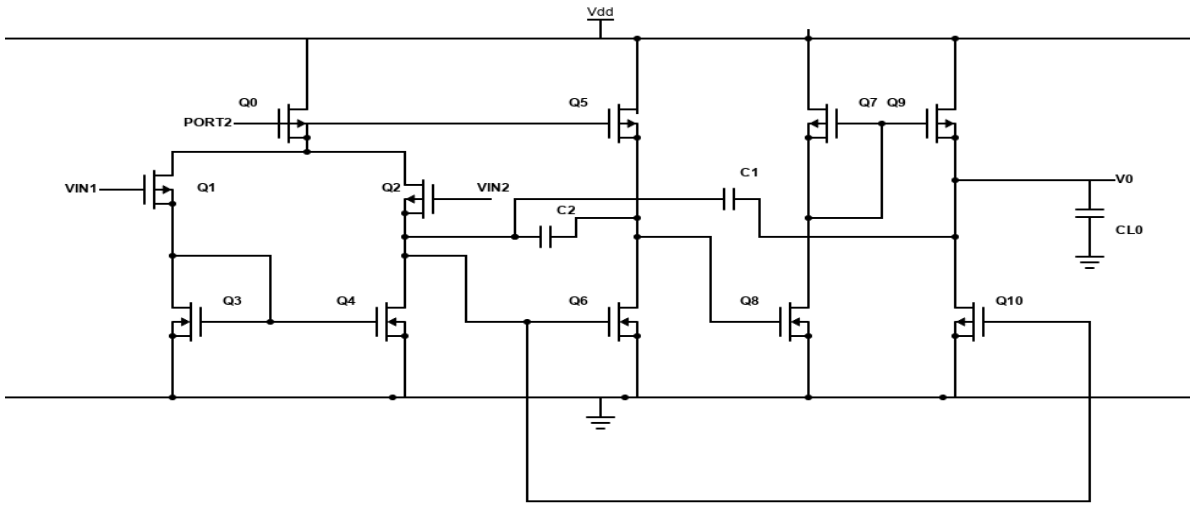


Figure 1: Three stage OTA with reverse nested frequency compensation

Table 2: Main performance parameter

Technology	*45 nm*	*90 nm*
Supply voltage (mv)	500	900
Gain (dB)	77.9	104.7
UGB (MHz)	.610	7.0605
Phase Margin (Degrees)	61.56^0	60.78^0
Compensation capacitor (pF)	2	2.3
Current	200 nA	4 µA
Power dissipation	857.621 nw	53.89 µw
CMRR(dB)	56	76
PSRR (dB)	69.24	53.27
Offset voltage error (mv)	17.86	13.34
Input noise	1.005 µv/sqr(Hz)	587.46 nv/sqr(Hz)
FOMs	1422 MHz.pF/µw	298.7 MHz.pF/mw

Table 3(a): Monte Carlo analysis

Monte Carlo 45 nm	*Mean*	*Median*	*Standard deviation*
Gain	5.24	8.384	27.58
CMRR	51.98	53.5	5.067
PSRR	-67.31	-65.98	10.32
Power consumption	2.002µ	823.7n	1.754µ

Population Size -2000

Table 3(b): Monte Carlo analysis

Monte Carlo 90 nm	*Mean*	*Median*	*Standard deviation*
Gain	5.326	3.598	25.01
CMRR	43.2	44.02	27.11
PSRR	-36.52	-34.27	10.19
Power consumption	52.09µ	78.41µ	33.39µ

Population Size -2000

resulted in the drain current of Q1 and Q2 being set at 4 µA, while the drain current of the second and third stages reached 16 µA. Consequently, the total current consumption was successfully achieved at 52 µA. The dimensions of transistors are presented in a table. Figure 1 displays the simulated open loop frequency response of the amplifier. The DC gain is measured to be 104.7 (dB). The bandwidth product of the amplifier was measured to be 7.065 MHz, while the phase margin was determined to be 61.56^0.

Experimental Result

The transconductance of all the transistors for both technologies is mentioned in Tables 1(a) and 1(b) All the experimental outcomes performed in to the 45 and 90 nm cadence virtuoso environments for both technologies, respectively, are mentioned in Table 2 and Figure 2 shows the graphical representation of different performance parameter for both the technology. After applying a supply voltage is 1 mv V_{PP} in both technologies, the transient response is 500 and 900 mv in. For lower values of supply voltage, i.e. 500 and 900 mv, 77.9 and 104.7 dB gain is achieved, where 2 and 2.3pF of compensation capacitor is used for achieving the phase margin of 61.56^0 and 60.78^0 for both the technologies, which is our required phase margin for this lower value of compensation capacitor. The values of the compensation capacitor is further reduced by increasing the current of the second and third stages, respectively but the circuit will consume more power so there is trade-off in between the compensation capacitor (phase margin) and power consumption. Power consumption is 857.62 nw and 53.89 µw for both technologies, respectively.

Monte Carlo Analysis

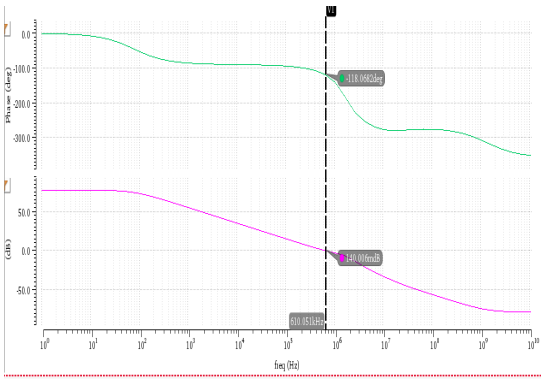
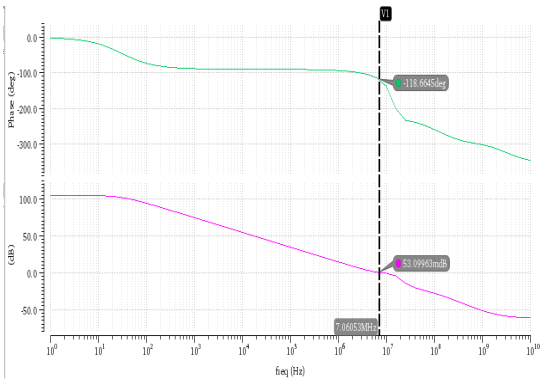
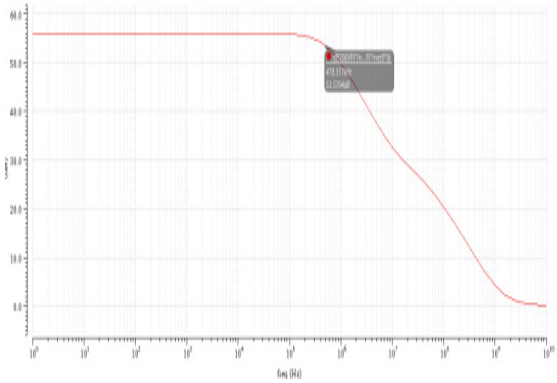
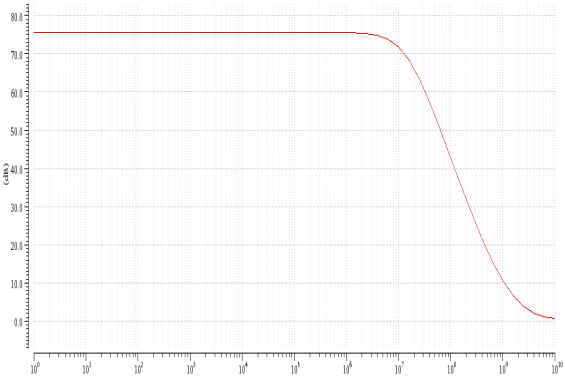
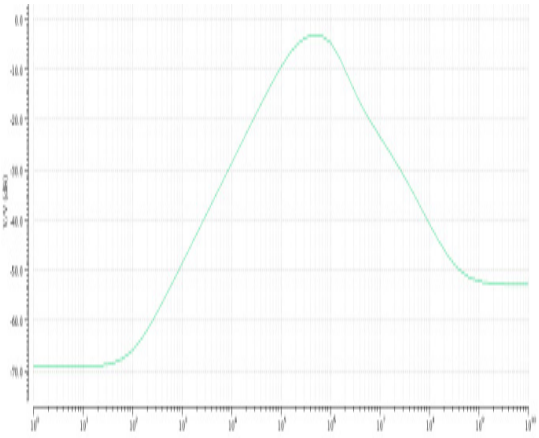
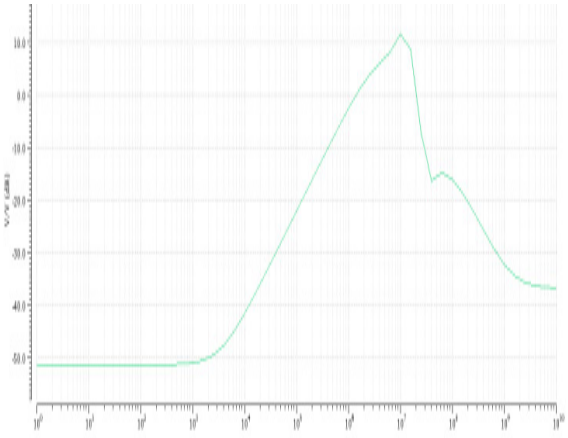
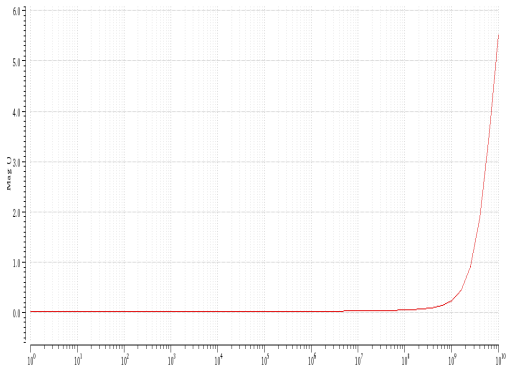
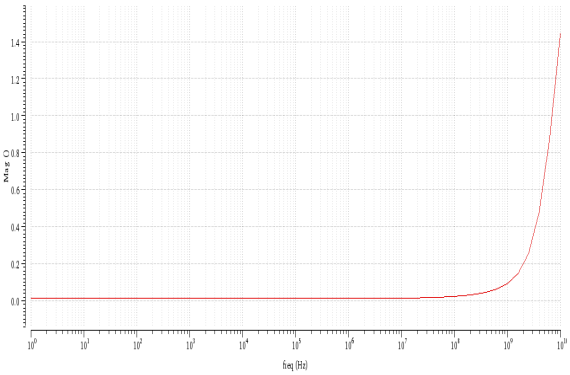
Monte Carlo simulation is a computational technique that leverages statistical distributions to realistically mimic

Table 4(a): Corner analysis

Corner analysis 45 nm	*Min*	*Max*	*Mean*	*Median*	*Standard deviation*
Gain	32.15	77.44	55.18	53.21	10.97
Phase	33.4	82.9	66.38	69.09	11.02
CMRR	38.67	59.07	51.98	53.5	5.067
PSRR	-88.06	-30.07	-51.75	-50.08	13.37
Power consumption	11.04 nw	22.02 µw	4.906 µw	857.6 nw	6.789 µw

Table 4(b): Corner analysis

Corner analysis 90 nm	Min	Max	Mean	Median	Standard deviation
Gain	6.412	104.8	49.85	50.78	26.13
Phase	60.68	113.9	79.18	79.53	17.29
CMRR	4.347	98.54	62.04	74.94	30.94
PSRR	68.81	7.24	-39.34	-51.47	26.19
Power consumption (µw)	21.26	105	59.48	54.81	23.48

	45 nm	90 nm
Gain and phase		
	(a)	(a)
CMRR		
	(b)	(b)
PSRR		
	(c)	(c)
Offset voltage error		
	(d)	(d)

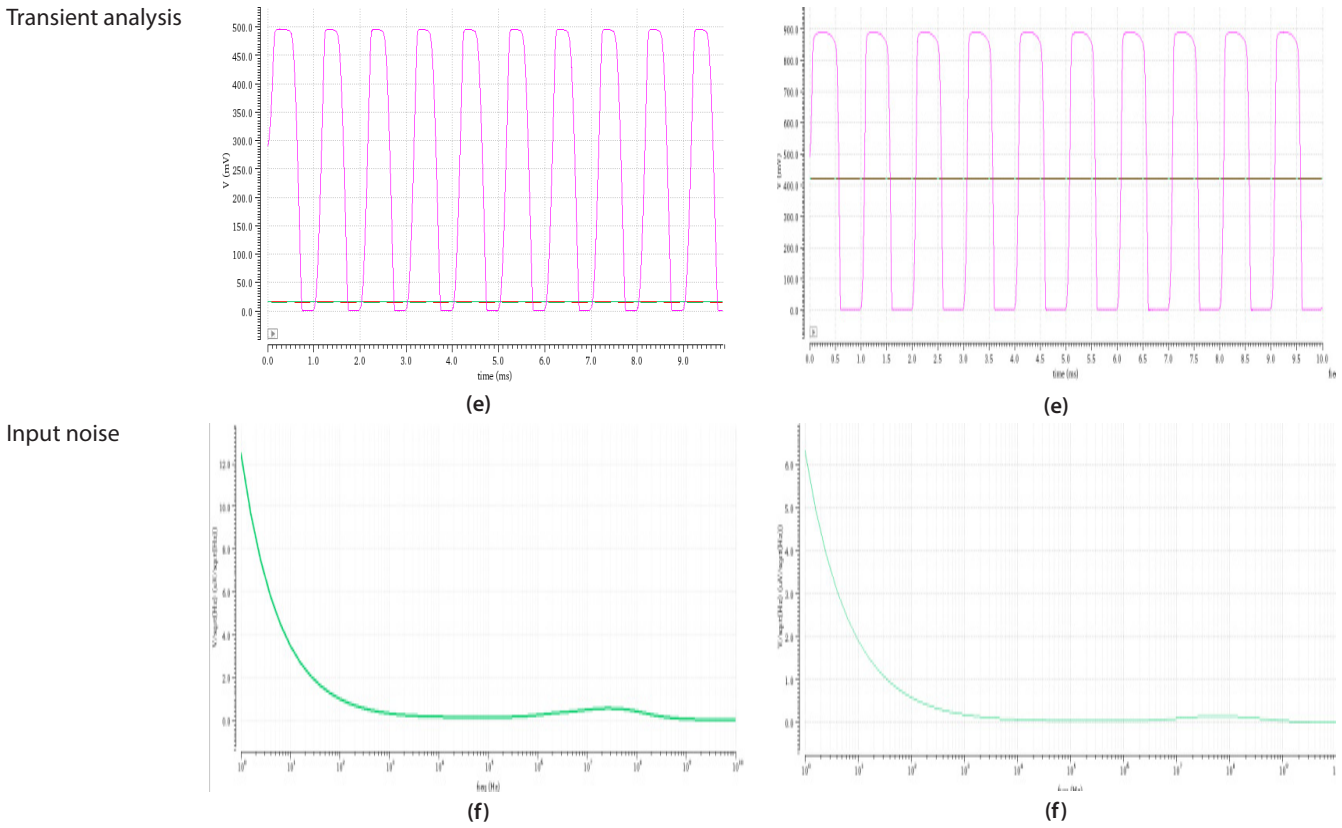


Figure 2: Graphs for different performance parameter

the effects of mismatching and process variation. Each parameter is stochastically determined using a statistical distribution model for every simulation iteration. Through the utilization of this research, it is possible to ascertain the geographical area in which our circuit will exhibit the highest frequency of operation. The three-stage CMOS OTA is subjected to a Monte Carlo simulation to evaluate its gain, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and power consumption. The simulations were conducted with a total population size of 2000 individuals. The statistical measures of mean, median, and standard deviation for the parameter are presented in Tables 3 (a and b), whereas Figure 3 displays a histogram illustrating the distribution of the various parameters.

Corner Analysis

While simulating a circuit with sets of parameter values that represent the most extreme variation in a manufacturing process, corner analysis offers a convenient technique to measure circuit performance. Corner analysis results can be compared to the permissible performance value range for each set of parameter values. We can make sure that the circuit has the highest yields feasible, so that every combination of parameters yields respectable results. The precise values of the process variables can be used to compute the yields for a fictitious manufacturing process. However, in actual manufacturing processes, process variables are subject to manufacturing tolerance; they unpredictably fluctuate in the direction of their ideal values. The circuit's overall yields are unknown as a result of the random changes for all of the components combined. Corner analysis examines the performance result produced by the most severe variations in process, voltage, and temperature values (the corners) that are anticipated. With this knowledge, you may assess whether the circuit's performance requirements will be met, even when random process variation combines in the most unfavorable ways.

Tables 4 (a and b) presented here in depict the process corner analysis of a three-stage CMOS OTA built for diverse performance parameters at both 45 and 90 nm technology nodes. In the nominal scenario, all the transistors inside the circuit are operating at their designated speed. The characteristics that are simulated in corner analysis are gain, phase, CMRR, PSRR, power dissipation, with temperature, supply voltage, and compensating capacitor as variable factors.

Environment set for 45 nm

Temp- 0, 27, 80
VDD- 400, 500, 600 m
CC1- 1, 1.5, 2 pF
CC2- .4, .5, .6 pF

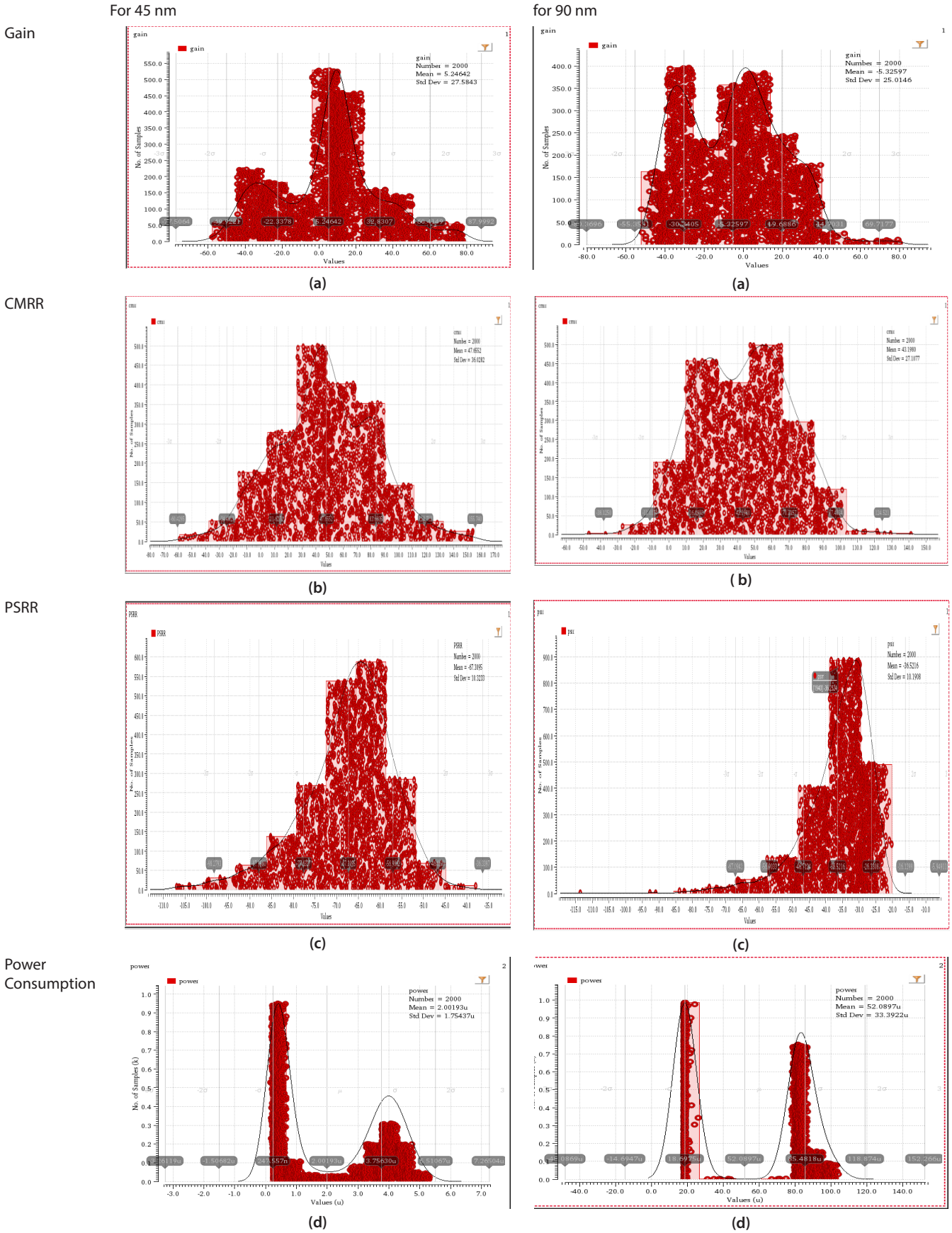


Figure 3: Histogram representation for Monte Carlo analysis for different performance parameter

Table 5: Comparative Analysis of different parameters in Respective years

Author	*A.D. Grasso*	*Sau Siong Chong*	*Mortaza Mojarad*	*Alfio Dario Grasso*	*Hamed Aminzadeh*	*Yi Xie*	*Sajad Golabi*	*Chuan Qinn*	*Gianluca Giustolisi*	*Gianluca Giustolisi*	*Hamed Aminzadeh*	*Siwan Dong*	*Shub-in Liu*	*Mehdi Zahrfe Kr*	*Francesco Centurelli*	*Joseph Riad*	*Farshad Alizadeh Arandin*	*This work*	
Year of publication	2007	2012	2013	2014	2015	2015	2015	2016	2016	2018	2018	2018	2018	2019	2020	2020	2020	2023	2023
Technology (nm)	500	65	90	65	90	65	90	65	65	65	90	180	65	180	130	130	90	45	90
Supply voltage (V)	3	1.2	.9	1	1.2	1.2	1.2	1.2	1	1	1.2	1.2	1.2	1.8	1	1	1.2	.5	.9
Dc gain (dB)	109	100	92.1	91	100	101.1	72	100	-	99.5	110	100	72.9	112	120	83.46	81.6	77.9	104.7
Power	.255 mw	.0204 mw	55.2 µw	.08 mw	80 µw	1.56 mw	2.5 mw	.04 mw	90 µw	19 mw	-	23 µw	-	.285 mw	16.7 µw	185 µw	3.25 mw	857.61 nw	53.89 µw
GBW (MHz)	2.4	2	15.1	19.06	1	330	121	.62	14.66	1.35	4.65	6.5	2.410	14	24.8	1.7	193.6	.610	7
Slew rate (v/µs)	1.95/ 1.8	.65	1.28	1.45	.19	266.3	487.9	.19	-	.85/ .97	1.71	.83	17.25	.8	10	.17	327.3	-	-
Phase margin	580	-	750	590	-	580	63.80	580	67.30	72.80	570	48.20	82.60	860	730	82.360	61.80	61.560	60.780
CMRR (dB)	79	-	-	-	-		-	-	-	-	-	-	-	-	-	-		56	76
Settling time (%)	497/ 560	-	870/ 433 ns@ 1	-	-	9.3 ns	75ns @.02	-	30.1/ 27.6 ns@ 1	431/ 493 100 mV (ns)	.52/.45 us @.1	-	1.4 ns 1	-	117/ 105 ns	.89 us @ 1	9.1 ns @ 1	-	-
Current (µA)	85 (µA)	17 µA	61 µA	80 µA	66 µA	-	-	50 µA	10 µA	19.1 µA	17 µA		10.6 mA	-	-	112 µA	-	200 nA	4 µA
Input voltage noise	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	-	1.005 uv/ sqr (Hz)	587.46 nv/sqr (Hz)
FOM (MHz. pF/ mw)	4706 FOMS	49020 FOMS	273551 FOMS	238250 FOMS	12500 FOMS	1057 .7 FOMS	96.8 FOMS	88571 FOMS	-	-	113 970 FOMS	1587 00 FOMS	382.5 FOMS	10.76 FOMS	1485 FOMS	4.63 GB. CL/ (IDC area) MHzpF / mA· µm2	125.32 FOMS	1422 MHz.pF/ µw	298.7
FOM (v/µs. pF/ mW)	3529 FOML	15931 FOML	23188 FOML	18125 FOML	23750 FOML	853.5 FOML	390.3 FOML	-	-	-	419 12 FOMS MHz. pF/ mw	20176 FOMS MHz. pF/mw	273.8 FOML	.61 FOML	598 FOMS nHz/ pF/mw	.87 SR.CL/ (IDC. area) h Vµs.pF/ mA.µm2	211.4 FOML v/µs. pF/mv	-	-
PSSR (dB)	75	-	-	-	-	-	-	-	-	-	-	-	-	-	-		-	69.24	53.27
Estimated Area (mm2)	-	-	-	-	-	-	-	.008	-	-	-	.006	-	. -	-	.006	-	-	-

Environment set for 90 nm

Temp- 0, 27, 80
VDD- 800, 900, 1000 m,
CC1- 1.2, 1.8, 2.4pF
CC2- .4, .5, .6pF

Conclusion

The basic RNMC topology is presented for different technologies i.e., 45 and 90 nm. The desired gain, phase, CMRR, and PSRR are achieved with lower supply voltage, bias current, power consumption, and output condition set for $V_{DD}/2$. The design and implementation of compensation techniques necessitate a straightforward approach. Given that only passive components are necessary. Specifically, achieving optimal performance necessitates using only two compensation capacitors, both of which should have lower values. Ultimately, a comprehensive analysis is conducted to compare the various options. The selection of transistor size and biasing for the second and third stages in all technologies is determined in order to achieve a compensating capacitor value of around 2 pF.

In (*Leung, K.N.,2001*) and (*Grasso, A.D.,2007*) nulling resistor R_C is used because nulling resistor blocks feed forward paths and it can prevent output impedances of the first stage form being pulled down by compensation capacitor at high frequency. Consequently the nulling resistor improves the phase margin by reducing the first stage gain drop at high frequencies *(Ho, K.P., 2003*). Although this particular work presented here is exploited by making nulling resistor R_C=0. Further Monte Carlo analysis result of which is mentioned in Table 3 (a and b) and histogram representation of same is shown in Figure 3 for different performance parameter and Corner analysis result of which is mentioned in Table 4 (a and b) for different variable is performed.

Table 5 represents the comparative study for performance parameters of respective years and work done in this paper. 104.7 dB of gain is achieved for .9 v of power supply which is comparatively good gain for such a low value of power supply in 90 nm technology. Power consumption for this amplifier is 53.89 μw for 4 μA of biasing current, comparable to all the papers mentioned in Table 5.

77.9 dB of gain for .5 v of power supply is achieved in 45 nm technology this amplifier is biased for 200 nA of current power consumption for this circuit is 857.62 nw, power consumption is lowest among all the work mentioned in Table 5.

Further by (*Ho, K.P., Chan, 2003*) and (*Leung, K.N. 2001*) a comparative study is shown for NMC and RNMC with voltage buffer as feedback path with nulling resistor and without nulling resistor where considerable improvement in overall parameters is tabled and makes available room for future work for the OTA presented in this work, will be implemented with the calculated value of nulling resistor R_C as mentioned (*Grasso, A.D., 2007*) and providing comparative analysis for improvement in overall parameter.

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