The Scientific Temper
OCTOBER 2026 Vol. 17 (10): 7102-7111
ISSN: 0976-8653, E-ISSN: 2231-6396
DOI: 10.58414/SCIENTIFICTEMPER.2026.17.10.2571
A WEB OF SCIENCE JOURNAL

RESEARCH ARTICLE

Low-Power Tuneable Operational Transconductance Amplifier Low-Pass Filter at 90nm CMOS

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ABSTRACT

Analog circuits for biomedical applications often have low power and low voltage requirement for processing low-frequency and low-amplitude EEG, ECG, and EMG signals. Existing Operational amplifier (Op-Amp) based analog circuits suffer from high power consumption and lack electronic tuneability. Consequently, Operational Transconductance Amplifiers (OTAs) have emerged as a suitable replacement, offering lower power consumption, better linearity, and carries external bias control connection to tune circuital parameters. In this regard, this work showcases a complementary-input, fully differential, CMOS, OTA based low-pass filter for low power biosignal processing application. The filter is designed with the help of 90nm CMOS technology and applies a bias voltage control technique in which tuning voltage regulates the bias current and transconductance through NMOS current sink transistor. At a voltage V_{bais}= 500 mV and supply voltage of 1V, the filter has achieved a maximum gain of 22.56 dB, a cut-off frequency of about 270.8 Hz, an input referred noise (IRN) of 665 nV/sqrt(Hz) and power consumption of only 32.91 µW which indicates that the low-frequency response can be effectively tuned by varying the bias voltage. Monte carlo simulation demonstrates negligible deviation of total power consumption against their respective mean value, establishing insensitivity of the filter to the process and mismatch variations. Compared to previously reported filters, the proposed filter offers a low cut-off frequency f_c , low input referred noise (IRN), low power consumption and provide a basis for selecting a bias condition for the low frequency biosignal applications.

Keywords *- OTA (Operational Transconductance Amplifier), Fully Differential OTA, Bias-Voltage Control, Low-Power CMOS.*

INTRODUCTION

The use of portable and wearable healthcare systems has increased the demand for compact and low-power analog circuits (Lou, Z., et al. 2026 & Xu, J., et. al. 2025). Biosignals such as EEG (electroencephalogram), ECG (electrocardiogram) and EMG (electromyogram) are generally small in amplitude and contain low-frequency information (Yan, F. and Liu, J., 2025; Liu, F. and Lorenzelli, L. 2024; Mehrabi Moghadam, Z., et al. 2025; Emon, M. Z. A., et al. 2024). Analog circuits used to process these signals require sufficient gain for proper signal amplification. At the same time, low noise, low power consumption, and low distortion are important for maintaining the signal quality and reliable operation (Kledrowetz, V., et al. 2023; Kulej, T., et. al. 2026; Lo, T.-Y., et al. 2007; Rezaei, F., et al. 2011).

The performance of CMOS operational transconductance amplifiers (OTAs) is dependent

Received: 5th October, 2026 **Accepted: 7th October, 2026** **Published: 28th October, 2026**

on the transistor operating point and bias conditions. In OTA-based continuous-time filters, the transconductance g_m directly influences the filter cutoff frequency, while the bias current affects power consumption (Moosaei, A., et al 2015; Maheshwari, S. and Pandya, J. P., et al. 2018; Kumngern, M., et. al. 2024). Therefore, varying the bias voltage or current provides an effective way to electronically tune the filter frequency response without changing the supply voltage (Yin, Y., et al. 2024; Choi, J., et al. 2023). Various CMOS OTA and electronically tunable filters have been previously reported in the literature for low-power and tunable analog signal-processing applications. (Kulej, T., et al 2024) presented a multiple-input fully differential OTA operating at a 0.5 V supply and evaluated its used in a fifth-order Chebyshev low-pass filter designed for bio-signal processing applications. The reported filter achieved a power consumption of 60 nW while operating at a 0.5-V supply voltage, with a total harmonic distortion of 0.97%. The Monte Carlo simulations, and temperature dependent evaluation were also done to assess the circuits performance under varying operating conditions. The OTA operated at a 0.4-V supply with power consumption below 30 nW, and its application as a low pass filter with a cutoff frequency of 250-Hz. (Khateb, F., et al. 2022) reported multiple input OTA-based filter designed to suppress noise and motion related disturbances in the biosignal acquisition, including low-pass and band-pass filtering functions for biomedical signal-processing applications. (Kumngern, M., et al. 2025) reported a tunable third order elliptic low-pass filter based on an OTA-C architecture, operating at a supply voltage of 450-mV for biosignal application. The reported filter consumed 40.5 nW of power, and achieved a cutoff frequency of 112.9 Hz, and a dynamic range reached 66.7 dB under 1% THD condition. Monte Carlo analysis and PVT analysis have also been performed. Other a low-voltage OTA-C and Gm-C filter techniques have also been reported for biomedical and low-frequency signal-processing applications (Phatsornsiri, P., et al. 2025; Srinivasagan, R., 2025; Ram Babu, R., Et al. 2017).

In this work, a fully differential CMOS OTA is configured as a low-pass filter for the low-frequency biosignal-processing applications. The proposed architecture employs complementary PMOS and NMOS differential input stages for differential signal processing. Current-mirror and current-steering structures are used to establish the signal-processing paths and differential output operation. A controllable NMOS current-sink transistor is incorporated to provide bias control. By varying the voltage $V_{bias,}$ applied to this transistor, the operating current and small-signal transconductance g_m of given OTA can be controlled, resulting in a tunable filter response. The influence of the bias voltage on gain, cutoff frequency, noise, total harmonic distortion, and power consumption is investigated.

The proposed circuit is designed in Cadence Virtuoso with a 90-nm CMOS technology, at supply voltage of 1-V. The bias voltage is varied from 100 mV to 900 mV to investigate its effect on the main circuit parameters. DC, AC, transient, noise, harmonic-distortion, and Monte Carlo analyses are performed under different bias conditions. The investigated parameters include gain, cutoff frequency, noise, total harmonic distortion, and power consumption.

PROPOSED MODIFIED OTA ARCHITECTURE

The proposed OTA based filter, implemented using 90-nm CMOS technology, is reported in Figure 1. It uses bias-voltage-controlled technique to optimize parameters at a 1 V supply voltage and 500 mV bias voltage.

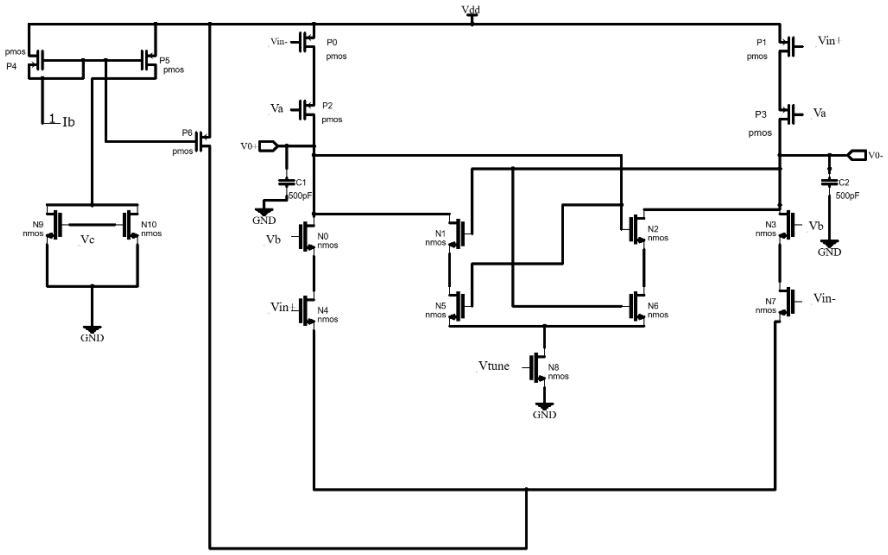


Figure 1. Proposed fully differential CMOS OTA-based low-pass filter with bias control.

The filter uses complementary PMOS and NMOS differential input stages where input signals are applied at V_{in+} and V_{in-} through PMOS transistor P_1 and NMOS transistor N_7 while bias voltage V_a and V_b controls the active load and gain stages. The PMOS transistors from P_0 to P_6 forms upper current mirror network, NMOS transistor from N_0 to N_7 shows differential amplifier, current-steering and gain stages, transistor N_8 represents controllable current sink device, capacitor C_1 and C_2 (=500pF) at input and output terminals is used for capacitive loading respectively while output is taken across V_O.

Differential current mirrors and output branches are used to obtain a fully differential output. The voltage V_{bias} applied at the gate terminal of NMOS transistor N8, and this voltage changes the operating current of the associated transistor network. The circuit does not use a separate bias-voltage-controlled technique. Instead, the main control used in this work is bias-voltage control. The voltage applied to N8 is varied to change the transistor operating condition and the current in the corresponding bias path. This changes the small-signal operating point of the OTA and, consequently, affects parameters, such as cutoff frequency, gain, noise, and power-consumption. As the bias voltage changes, the current and transconductance of the associated devices can change. The resulting change in the OTA operating point affects the frequency response and power consumption. The simulated results are therefore presented for several bias-voltage values to show this behaviour.

The main technique used in the proposed circuit is bias-voltage-controlled tuning of the OTA operating point. This approach is simple because the variation in cutoff-frequency is obtained by changing the bias voltage applied to N8, while the supply voltage remains fixed at 1 V.

DESIGN METHODOLOGY

The dimensions of transistors and other details are precisely selected, shown in Figure 2, for low-voltage operation.

CIRCUIT PARAMETERS & BIAS CONDITIONS

V_a = 600 mV I_B = 250 nA
V_b = 500 mV C_L = 500 pF
V_Bias = 0.1 to 0.9 V
V_c = 400 mV

Transistor	W / L
P0 - P1	500 n / 180 n
P2 - P3	300 n / 180 n
P4, P5	500 n / 180 n
P6	2 µ / 180 n
N0 - N10	1 µ / 180 n

Figure 2. Circuital Parameters and bias condition

The main variable in the study is the bias voltage applied to transistor N8. This voltage was varied from 100 mV to 900 mV while the supply voltage and other simulation conditions were kept unchanged.

For each of the bias-voltage values, the DC operating-point analysis has been done to check the transistor operating conditions. AC analysis was then used to obtain the voltage gain and cutoff frequency. Transient analysis has been used to observe the time domain response. Noise analysis was used to obtain the noise power spectral density. These analyses were repeated for the selected bias-voltage values.

The results for different bias voltages were compared with other State-of-Art designs to understand how the bias voltage changes the main performance parameters of the OTA.

RESULTS AND DISCUSSIONS

The transient response is evaluated using 1 KHz sine wave, with an input signal of 1 mV peak-to-peak (p-p). The simulated output waveform, shown in Figure 3, has an amplitude of approximately 1.3 mV (p-p). The output amplitude is greater than the input amplitude, showing amplification under the performed simulation condition.

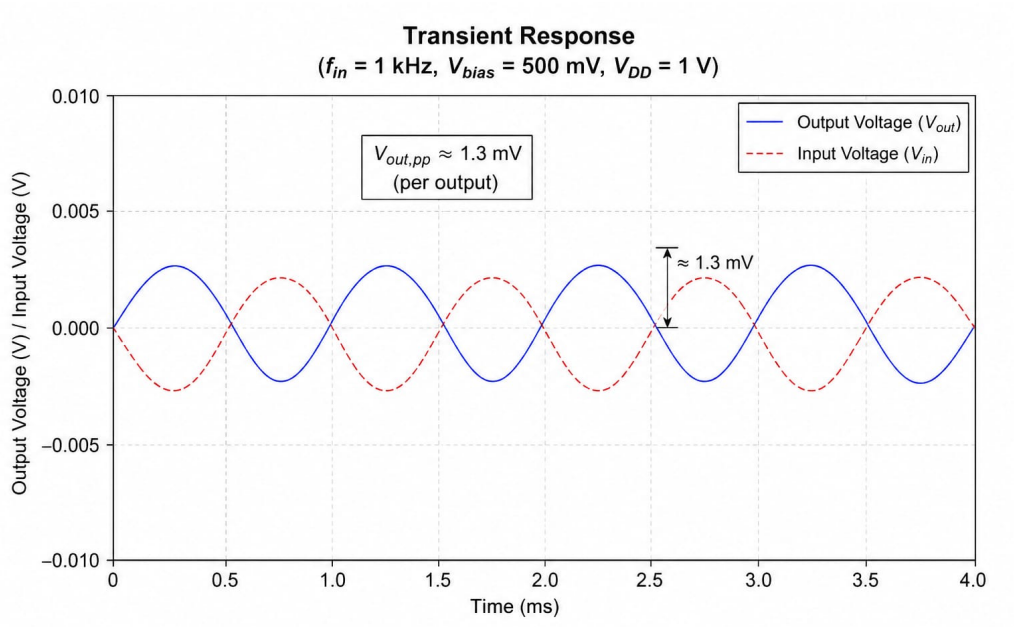


Figure. 3. Transient response of proposed CMOS OTA circuit.

The DC gain and frequency- dependent behaviour are also studied for different bias voltages. At a 500-mV bias voltage, the simulated DC gain is 22.56 dB, which corresponds to about 13.43 V/V which was highest among different bias voltages shown in Figure 4. The corresponding 3 dB cut off frequency is approximately 270.8 Hz, and the unity-gain bandwidth (UGB) is approximately 3.679 kHz.

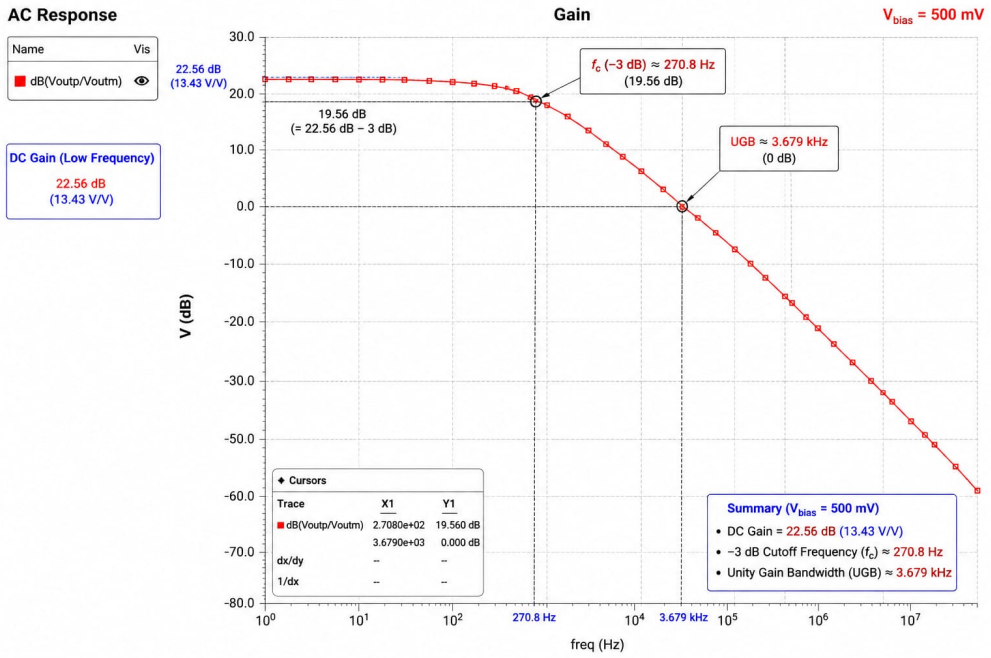


Figure 4. AC response of proposed fully differential, CMOS OTA based low-pass filter.

Figure 5 and 6 depicts the gain characteristics of OTA-based low-pass filter at bias voltages of 500 mV, 600 mV, and 700 mV and variation of total power consumption of circuit at different bias voltage respectively.

It is found that as the bias voltage is increased beyond 500mV, the gain decreases to approximately 19.91 dB (9.9 V/V), while the cutoff frequency increases to approximately 363 Hz. At 700 mV, the gain decreases further to approximately 15.70 dB (6.1 V/V), while the cutoff frequency increases to approximately 524 Hz.

These results show that the cutoff frequency and gain changes with the applied bias voltage which indicates that bias-voltage control can be used to adjust the low-frequency response without changing the 1 V supply voltage, however, practical operating point can be selected according to the required gain, cutoff frequency, noise, and power consumption.

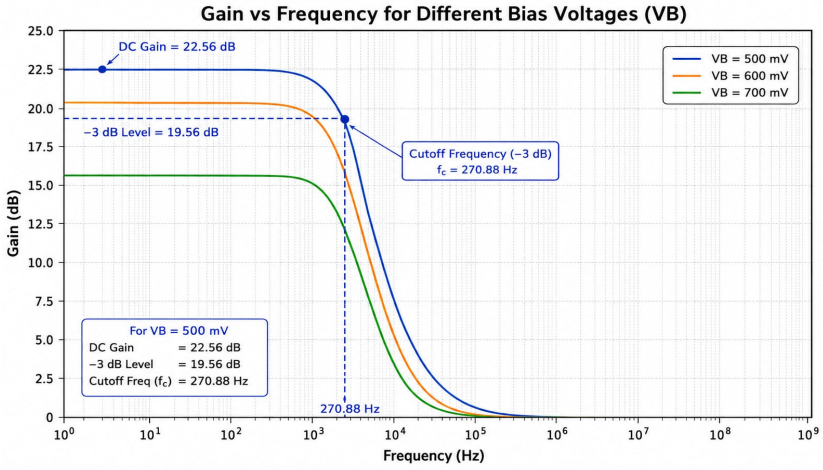


Figure 5. Gain variation with frequency under different bias voltage values.

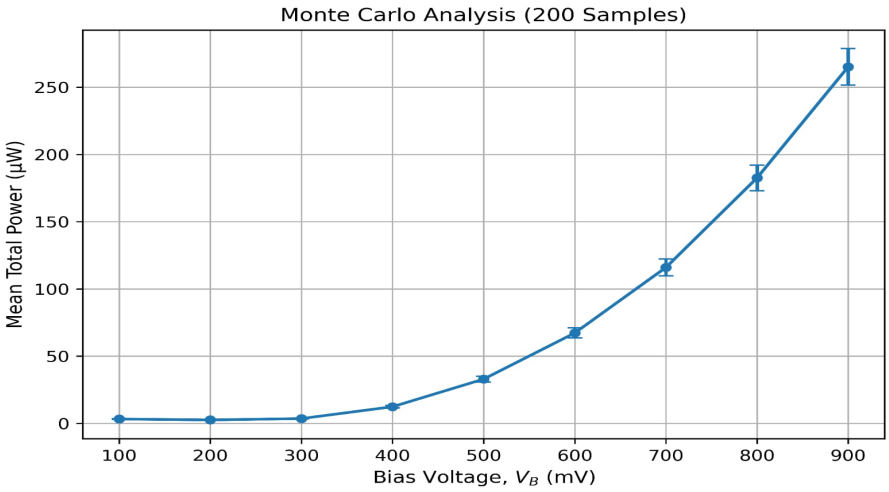


Figure 6. Monte Carlo analysis of total power consumption under varying bias condition.

Figure 7 represents the noise power spectral density (PSD) of the proposed circuit for bias voltage values of 500 mV, 600 mV, and 700 mV.

In the frequency range 1 Hz to 1 GHz, the simulated noise is higher at low frequencies, where flicker-noise effects are important, and becomes more nearly constant at higher frequencies as the white-noise contribution becomes more dominant. At 1 kHz, the simulated PSD values are approximately 5.09 pV²/Hz at 500 mV, 4.80 pV²/Hz at 600 mV, and 3.72 pV²/Hz at 700 mV.

At 700mV bias voltage, lowest value of PSD is obtained, however, power consumption increased simultaneously. This result shows that increasing the bias voltage can reduce the simulated PSD in the selected operating range and the bias voltage should be selected by considering both noise and power consumption.

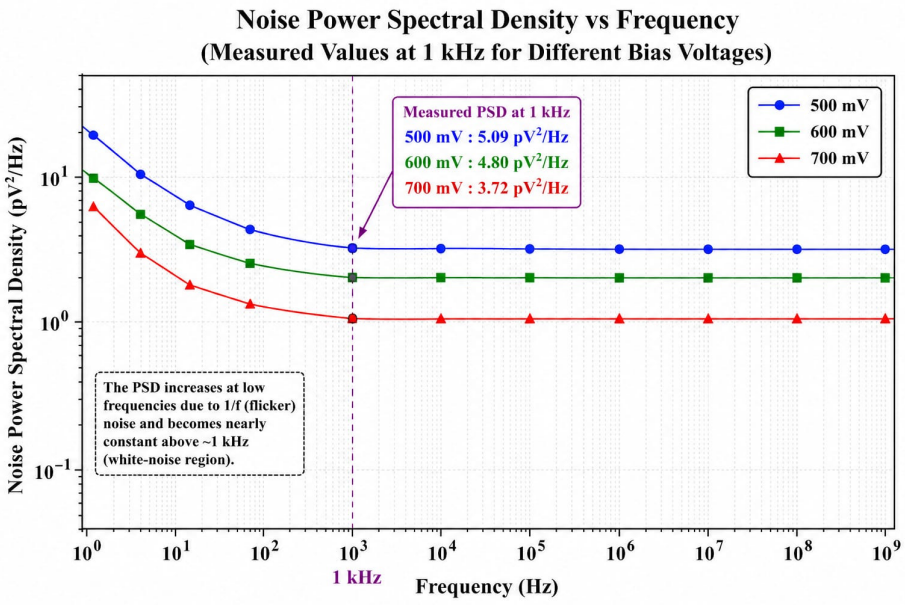


Figure 7. Noise PSD of the proposed circuit at different bias voltages.

Figure 8(a) represents the Monte Carlo analysis of total power consumption using 200 samples. The mean power consumption increased from approximately 3.26 µW at 100 mV to 265.2 µW at 900 mV while the standard deviation increased from approximately 357 nW to 13.49 µW. This indicates that the mean power consumption increased as the bias voltage increased. The increase in power consumption with bias voltage is consistent with the increase in circuit current under the tested operating conditions. The larger standard deviation at higher bias voltages also represents a larger absolute variation in power.

Table 1. Monte Carlo results of total power consumption.

Bias Voltage V_B (mV)	Nominal Total Power (µW)	Yield (%)	Minimum (µW)	Maximum (µW)	Mean (µW)	Standard Deviation
100	3.30	100	2.48	4.44	3.26	357 nW
200	2.60	100	2.12	3.07	2.59	188.9 nW
300	3.58	100	2.94	4.52	3.59	308.1 nW
400	12.38	100	10.46	14.93	12.41	956 nW
500	32.91	100	28.57	38.34	32.96	2.10 µW
600	67.22	100	59.16	76.93	67.28	3.80 µW
700	116.70	100	103.00	132.00	116.00	6.33 µW
800	182.50	100	161.70	205.60	182.60	9.53 µW
900	265.00	100	235.00	297.00	265.20	13.49 µW

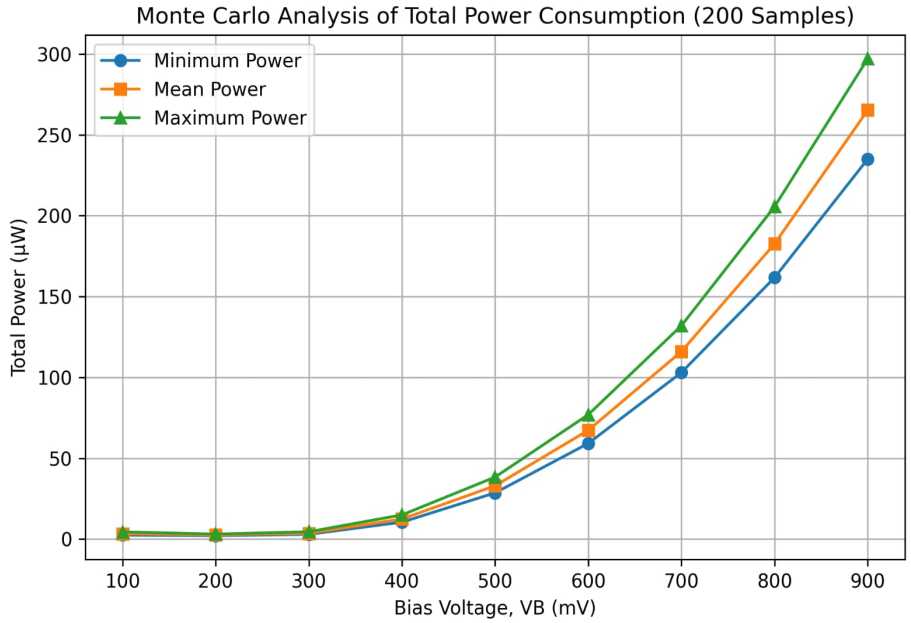


Figure 8(a). Monte Carlo analysis of total power consumption using 200 samples

Figure 8(b) shows the Monte Carlo distribution of total power consumption at a bias voltage of 500 mV using 200 samples.

The analysis includes process and mismatch variations. The distribution shows how the simulated power consumption varies around the nominal operating point for the selected samples. The result gives the spread of power consumption at 500 mV under the simulated variation conditions. It provides an additional check of the power-consumption variation at the selected operating point.

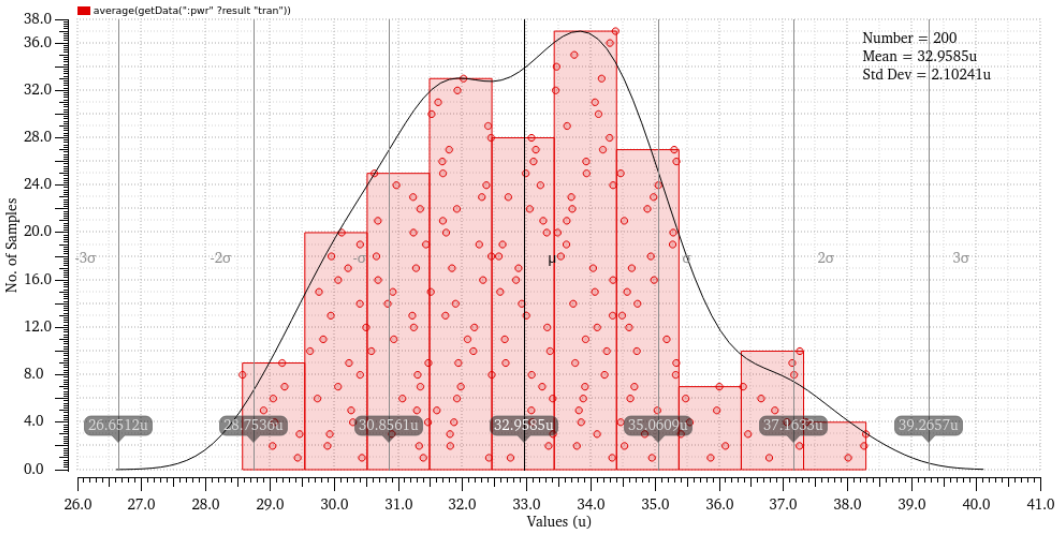


Figure 8(b). Monte Carlo analysis of total power consumption at 500 mV bias voltage.

Total harmonic distortion (THD) was calculated using the transient analysis for bias voltages from 100 mV to 900 mV. The THD is approximately 1.058% over most of the investigated bias-voltage range. At 900 mV, the THD is approximately 1.05966%. The change in THD over the investigated range is small. This indicates that the simulated harmonic distortion is not strongly affected by the bias-voltage change under the selected test conditions.

The THD results therefore show similar simulated linearity for the tested bias voltages. The result is limited to the input signal and simulation conditions used for the THD analysis. The pre-layout of the fully differential CMOS OTA us shown in Figure 9 using 90-nm GPDK090 CMOS technology. The layout dimensions are approximately 9.52 µm × 9.52 µm, giving an area of about 90.63 µm². The layout contains the OTA core and the required input, output, power, and bias connections. External voltage sources, current sources, and capacitors used during simulation were not included in the physical layout.

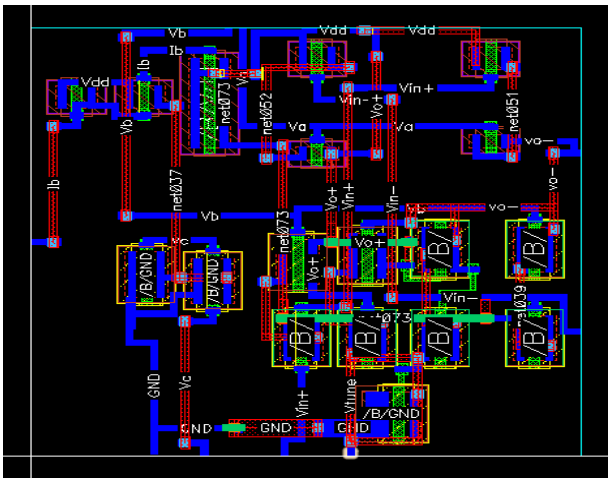


Figure 9. Layout Design of filter (9.52 µm × 9.52 µm)

Table 2 compares proposed filter with the previously published designs. The comparison includes technology, order, supply voltage, DC gain, cutoff frequency, power consumption, THD and IRN. This filter exhibits higher DC gain than (Ismail, S. H., et. al. 2011; Kumar, R., et. al. 2016; Póvoa, R., et. al. 2020), lower cut-off frequency than (Ismail, S. H., et. al. 2011; Elamien, M. B., et. al. 2018; Kumar, R., et. al. 2016; Póvoa, R., et. al. 2016; Póvoa, R., et. al. 2020), and lower power dissipation than (Ismail, S. H., et. al. 2011). These characteristics are essential for the low-frequency biomedical applications. Key contribution of the present work is the attainment of tuning in the low-frequency response with the applied bias voltage.

Table 2: Comparison of the proposed filter with previously published designs

Parameter	Ismail, S. H., et. al. (2011).	Elamien, M. B., et. al. (2018)	Póvoa, R., et. al. (2020)	Kumar, R., et. al. (2016)	Póvoa, R., et. al. (2020)	Proposed Work
Technology	180 nm	90 nm	90 nm	180 nm	130 nm	90 nm
Order	3	3	4	—	2	1
Operating voltage	0.9 V	1 V	1.2 V	0.85 V	0.9 V	1 V
DC Gain	5–21 dB	—	—	2 dB	7 dB	22.56 dB
Cutoff frequency	>1 MHz	4.57–12.59 MHz	814Hz–12 MHz	500 Hz	415 Hz	270.8 Hz
Power consumption	411.6 µW	1.16 mW	11.83 mW	1.2 µW	0.55 µW	32.91 µW
Total Harmonic Distortion (THD)	<–40 dB	—	<–60 dB	—	–60 dB	1.058%
Input Referred Noise (IRN)	167 nV at 1 MHz	—	293.6 nV	23 µV	—	665 nV at 1 kHz

CONCLUSION

A bias-voltage-controlled OTA low-pass filter is designed using 90nm CMOS technology. The circuit work at a 1 V power supply and the main control variable is the bias voltage applied to transistor N8, which was varied from 100 mV to 900 mV.

At 500 mV bias voltage, the simulated gain is 22.56 dB, the cutoff frequency is approximately 270.8 Hz, and the unity-gain bandwidth is approximately 3.679 kHz. The power consumption at this operating point is approximately 32.91 µW, while the simulated THD is close to 1.058%. When the bias voltage is increased, the cutoff frequency also increases in the selected range. The cutoff frequency is approximately 363 Hz at 600 mV and 524 Hz at 700 mV, while the gain decreases. Thus, the bias voltage affects both gain and cutoff frequency. Monte Carlo analysis with 200 samples was used to observe power-consumption variation under the selected process and mismatch conditions. The reported 100% yield is based on the acceptance criterion used in the simulation and should not be taken as a general reliability result.

The overall simulation demonstrate that the operating characteristics of the proposed OTA can be adjusted through bias voltage applied to N8. The main contribution of this work is the study of the resulting changes in gain, cutoff frequency, noise, THD, and power consumption.

Acknowledgment

We would like to express our sincere gratitude to the Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya for providing academic support and facilities during the research. We also appreciate the valuable suggestions and encouragement received during the design, simulation and analysis of the proposed circuit.

Conflict of interest: None

Source of support: None

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